R18

Code No: 156DF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year II Semester Examinations, March - 2024

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	What are the different operating regions for an MOS transistor?	[2]
b)	Compare CMOS and Bi-CMOS.	[3]
c)	List the salient features of subsystem lay out.	[2]
d)	What are scalable design rules and list its disadvantages.	[3]
e)	Define Fan-in and Fan-out.	[2]
f)	Discuss the inverter delay and propagation delay.	[3]
g)	What are zero detectors? What are their applications?	[2]
h)	Write a short note on shift registers.	[3]
i)	What are the advantages of CPLDs?	[2]
j)	Discuss the applications of FPGA.	[3]

PART – B

(50 Marks)

2.a)	Explain in detail the fabrication process of n-MOS transistor with neat diagrams.	
b)	Explain the operation of CMOS inverter with a logic diagram.	[5+5]
	OR	
3.a)	Derive the relation between drain to source current versus drain to source voltage in non-saturated and saturated region.	
b)	Determine the Pull-up and Pull-down ratio of for NMOS inverter through pass transistors.	[5+5]
4.a)	Discuss about the CMOS design style.	
b)	Draw the circuit diagrams and the corresponding stick diagrams for nMOS inverter.	[4+6]
	OR	
5.a)	What is stick diagram and explain about different symbols used for components in Stick diagram.	
b)	Design a stick diagram for NMOS EX-OR gate.	[5+5]

6.a) Implement the realization of NAND and NOT gates using PMOS.
b) Explain the effect of wiring capacitance on the performance of a VLSI circuit. [5+5]

OR

7.a) Realize the 2-i/p NAND gate using PMOS and CMOS technologies.
b) How switch logic can be implemented using Pass Transistors? Explain. [6+4]

8.a) Discuss the implementation of ALU functions with an adder.
b) Write a detailed note on the Parity generator with structured design. [5+5]

OR

9.a) Discuss the implementation of synchronous counter.
b) Explain briefly about the structure of static RAM cell. [5+5]

10.a) Explain the principle and operation of PAL.
b) Distinguish PLA, PAL, FPGA and standard cell. [5+5]

OR

11.a) Illustrate the principle and operation of CPLD.
b) Explain the various approaches in CMOS testing. [5+5]

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